CLAIMS

1. A system comprising:

a first bus master;

a second bus master;

a first bus arbiter coupled to the first and the second bus masters;

a second bus arbiter coupled to the first and the second bus masters;

a first bus slave coupled to the first bus arbiter, the first bus master requesting a first data operation on the first bus slave via the first bus arbiter, the first data operation being performed during a first period; and

a second bus slave coupled to the second bus arbiter, the second bus master requesting a second data operation on the second bus slave via the second bus arbiter, the second data operation being performed during the first period.

2. A system comprising:

a first bus master configured for generating a first arbitration request and a first target address on which a first data operation is to be performed, the first target address containing first address information;

a second bus master configured for generating a second arbitration request and a second target address on which a second data operation is to be performed, the second target address containing second address information;

a first bus arbiter coupled to the first and second bus masters, the first bus arbiter receiving the first and the second target addresses from the first and the second bus masters, respectively, wherein the first arbitration request is provided to the first bus arbiter by decoding the first address information;

a second bus arbiter coupled to the first and the second bus masters, the second bus arbiter receiving the first and second target addresses from the first and the second bus masters, respectively,

wherein the second arbitration request is provided to the second bus arbiter by decoding the second address information;

a first bus slave coupled to the first bus arbiter, the first bus master requesting the first data operation on the first bus slave via the first bus arbiter, the first data operation being performed during a first period; and

a second bus slave coupled to the second bus arbiter, the second bus master requesting the second data operation on the second bus slave via the second bus arbiter, the second data operation being performed during the first period.

3. The system of Claim 2, further comprising:

a first gating logic coupled to the first master for receiving the first arbitration request and the first address information from the first master, and coupled to the first bus arbiter for providing the first arbitration request to the first bus arbiter; and

a second gating logic coupled to the second master for receiving the second arbitration request and the second address information from the second master, and coupled to the second bus arbiter for providing the second arbitration request to the second bus arbiter.

4. The system of Claim 2, further comprising:

a first gating logic coupled to the first master for receiving the first arbitration request and the first address information from the first master, and coupled to the first bus arbiter for providing the first arbitration request to the first bus arbiter, wherein the first gating logic includes a first pipeline manager when the first bus arbiter is capable of performing pipeline operations; and

a second gating logic coupled to the second master for receiving the second arbitration request and the second address information from the second master, and coupled to the second bus arbiter for providing the second arbitration request to the second bus arbiter, wherein the second gating logic includes a second pipeline manager when the second bus arbiter is capable of performing pipeline operations.

5. The system of Claim 1, wherein the system is implemented on a semiconductor chip.

6. The system of Claim 2, wherein the system is implemented on a semiconductor chip.

7. The system of Claim 1, wherein the system adopts a processor local bus (PLB) protocol.

8. The system of Claim 2, wherein the system adopts a processor local bus (PLB) protocol.

9. The system of Claim 1, wherein the first and the second data operations each includes one of read and write operations.

10. The system of Claim 2, wherein the first and the second data operations each includes one of read and write operations.

11. The system of Claim 1, wherein the first period contains one or more bus clock cycles in the system.

12. The system of Claim 2, wherein the first period consists of one or more bus clock cycles in the system.

13. The system of Claim 2, wherein the first bus arbiter receives the first target address during a second period, and wherein the second bus arbiter receives the second target address during the second period.

14. The system of Claim 2, wherein the first bus arbiter receives the first target address during a second period, wherein the second bus arbiter receives the second target address during the second period, and wherein the second period consists of one or more bus clock cycles in the system.

15. A system comprising:

a first bus master configured for generating a first arbitration request and a first target address on which a first data operation is to be performed, the first target address containing first address information;

a second bus master configured for generating a second arbitration request and a second target address on which a second data operation is to be performed, the second target address containing second address information;

a first bus arbiter coupled to the first and second bus masters, the first bus arbiter receiving the first and the second target addresses from the first and the second bus masters, respectively, wherein the first arbitration request is provided to the first bus arbiter by decoding the first address information;

a second bus arbiter coupled to the first and the second bus masters, the second bus arbiter receiving the first and second target addresses from the first and the second bus masters, respectively, wherein the second arbitration request is provided to the second bus arbiter by decoding the second address information;

a first bus slave coupled to the first bus arbiter, the first bus master requesting the first data operation on the first bus slave via the first bus arbiter, the first data operation being performed during a first period;

a second bus slave coupled to the second bus arbiter, the second bus master requesting the second data operation on the second bus slave via the second bus arbiter, the second data operation being performed during the first period;

a first gating logic coupled to the first master for receiving the first arbitration request and the first address information from the first master, and coupled to the first bus arbiter for providing the

first arbitration request to the first bus arbiter, wherein the first gating logic decodes the first address information to determine that the first target address is located in the first bus slave, thereby providing the first arbitration request to the first bus arbiter; and

a second gating logic coupled to the second master for receiving the second arbitration request and the second address information from the second master, and coupled to the second bus arbiter for providing the second arbitration request to the second bus arbiter, wherein the second gating logic decodes the second address information to determine that the second target address is located in the second bus slave, thereby providing the second arbitration request to the second bus arbiter.

16. The system of Claim 15, wherein the first gating logic includes a first pipeline manager when the first bus arbiter is capable of performing pipeline operations, and wherein the second gating logic includes a second pipeline manager when the second bus arbiter is capable of performing pipeline operations.

17. The system of Claim 15, wherein the system is implemented on a semiconductor chip.

18. The system of Claim 15, wherein the system adopts a processor local bus (PLB) protocol.

19. The system of Claim 15, wherein the first and the second data operations each includes one of read and write operations.

20. The system of Claim 15, wherein the first period contains one or more bus clock cycles in the system.

21. The system of Claim 15, wherein the first bus arbiter receives the first target address during a second period, and wherein the second bus arbiter receives the second target address during the second period.

22. The system of Claim 15, wherein the first bus arbiter receives the first target address during a second period, wherein the second bus arbiter receives the second target address during the second period, and wherein the second period consists of one or more bus clock cycles in the system.

23. A system comprising:

a plurality of bus masters including first and second bus masters;

a plurality of bus arbiters including first and second bus arbiters, each of the plurality of bus arbiters being coupled to the plurality of bus masters, wherein the first and the second bus arbiters are coupled to the first and the second bus masters, respectively; and

a plurality of bus slaves including first and second bus slaves, each of the plurality of bus slaves being coupled to one of the plurality of bus arbiters, wherein the first and the second slaves are coupled to the first and the second arbiters, respectively, the first bus master requesting a first data operation on the first bus slave via the first bus arbiter, the first data operation being performed during a first period, the second bus slave coupled to the second bus arbiter, the second bus master requesting a second data operation on the second bus slave via the second bus arbiter, the second data operation being performed during the first period.